French Patent 2,110,326

[Excerpt Translation]

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The present invention relates to a negative-resistance semiconductor device possessing a highly stable and reproducible memory characteristic and from which the stored information can be read any number of times.

According to the invention, à negative-resistance semiconductor contains at least four semiconducting regions with P-type or N-type conductivity; an insulating layer containing collector centers and which extends over at least three of said regions; and a trigger electrode constituting a control element disposed on said insulating layer, it being possible in this manner to enter into memory an input signal sent to the trigger electrode.

Other objects and advantages of the invention will become evident from the following description by referring to the drawings attached herewith, in which

Figure 1 is a cross-section of one embodiment of the invention,
Figure 2 is a graph of a static characteristic of the embodiment of Fig. 1,
Figure 3, finally, is a cross-section of another embodiment of the invention.

In Figure 1, reference numeral 1 indicates an N-type semiconducting substrate. Said substrate 1 contains regions 2 and 3 of type P. An electrode 4 is disposed on P-type region 2. A region 5 of type N is contained in region 3 of type P. An electrode 6 is disposed on region 5 of type N. On the surface of substrate 1 and between regions 2 and 3 of type P is formed an insulating layer 7 comprising numerous collector centers and a trigger electrode 8 which is also disposed in this zone.

The device thus constructed has a P-N-P-N structure between electrodes 4 and 5 and possesses a negative resistance characteristic in the same manner as does a thyristor. Thus, "on-off" control of the current flowing between electrodes 4 and 6 becomes possible by acting on the threshold voltage of the negative resistance with the aid of a voltage applied to trigger electrode 8. Moreover, because insulating layer 7 of the device contains numerous collector centers, a memory effect is produced as a result of the collection or trapping of electric charges. It is advantageous to indicate at this point of the description that it is possible to arrive at an equivalent result by replacing the N regions with P regions and the P regions with N regions.

We shall now describe a method of fabrication of the device shown in Fig. 1 and its operation. To create regions 2 and 3 of type P in the surface of a silicon substrate of type N, boron is diffused as an impurity (see Fig. 1). Also shown in Fig. 1 is a region 5 N' created in region 3 of type P by diffusing phosphorus in the latter. On the surface of substrate 1 thus treated, a film of silicon dioxide, SiO_2, is formed by thermal oxidation followed by a photoetching treatment to make the superfluous particles of the SiO_2 film disappear. Insulating layer 7 is thus obtained. Gold (Au) is diffused in insulating layer 7. Electrodes 4, 6 and 8 are formed by vapor deposition of aluminum. Under these conditions, a device with a P-N-P-N structure is obtained. Fig. 2 shows the static characteristic of said device. The figure is a curve showing the current as a function of the voltage, the application of the voltage to the trigger electrode 8 being considered as a parameter.

When a voltage is applied to trigger electrode 8, electric charges are injected into SiO_2 layer 7 and are trapped by the collector centers consisting of diffused gold (Au) atoms. As a result, insulating SiO_2 layer 7 remains charged even after the voltage applied to trigger electrode 8 has disappeared. Thus, an electric field, which may be attributed to the previously applied trigger voltage or, more exactly, to the trapped charges, continues to exist, and said field acts on the P-N junctions between region 2 of type P and substrate 1 of type N and between region 3 of type P and substrate 1 of type N. This persisting field serves to establish a threshold voltage between electrodes 4 and 6 which is entered into the memory. More precisely, if a certain voltage is applied to the trigger electrode 8, the device begins to be conductive at the corresponding threshold voltage between electrodes 4 and 6. However, the trigger field d_{μ} at this voltage persists, because the electric charges are always trapped by the collector centers of insulating layer 7 to set up an electric field. Thus, if a voltage is applied to the device between electrodes 4 and 6, but without applying a voltage to trigger electrode 8, the device begins to become conductive at a threshold voltage which is identical to that prevailing during the existence of a trigger voltage equal to that which was initially applied to trigger electrode 8. Under these conditions, a threshold voltage which depends on the trigger voltage is entered into the memory.

Fig. 3 shows another embodiment of the invention. In this case, the substrate is gallium arsenide (GaAs). The P and N regions which can be seen in Fig. 3 are formed by a technique involving growth from a melt.

In Fig. 3, a GaAs substrate of type N is indicated by reference numeral 9. Regions 10 and 11 of type P are formed on the two sides of substrate 9. A region 12 of type N is deposited on region 11 of type P. An electrode 13 is connected to region 10 of type P. Grooves 16a and 16b are formed by an appropriate technique. Insulating layers 15a and 15b are formed so as to coat grooves 16a and 16b or to cover substrate 5 of type N, region 11 of type P and region 12 of type N exposed in grooves 16a and 16b, as shown in Fig.3. Insulating layers 15a and 15b are formed by vapor deposition of SiO_2 with the addition of gold (Au). Electrodes 17a and 17b are formed on insulating layers 15a and

15b, respectively, mainly on the surfaces formed in or in the proximity of grooves 16a and 16b, which makes it possible to obtain two trigger electrodes of the MOS [metal oxide-silicon] type. An electrode 14 is formed on the surface of zone 12 of type N between grooves 16a and 16b. This gives a P-N-P-N device with a negative resistance characteristic. The current/device voltage characteristic, under the control of a voltage applied by the MOS trigger electrodes 17a and 17b, follows several curves like that shown in Fig. 2. In the embodiment of Fig. 3, collector centers are formed in SiO_2 insulating layers 15a and 15b, and such a P-N-P-N device has a memory effect similar to that of the P-N-P-N device of Fig. 1. More precisely, after suppression of the trigger voltage the device becomes conductive at a relatively low threshold voltage between electrodes 17a and 17b. The only difference between the device of Fig. 1 and that of Fig. 3 is that the latter has a GaAs substrate so that when the device is conductive, the regions of the P-N junctions are electroluminescent.

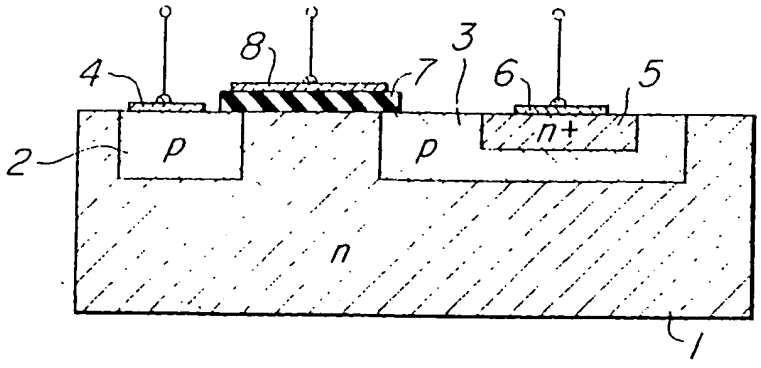
In the described embodiments, Si and GaAs are used as the substrate, respectively. Note, however, that equivalent results can be obtained by use of other semiconductive materials, such as GaP, Ge, GaPAs, InAs and CdS.

The memory effect which is also a very important characteristic of the invention can be attributed to the presence of collector centers which are distributed in the insulating layers. The doping with impurities of a level as deep as Au, Cu, Na, Fe and Ni or of lattice defects can be at the origin of such collector centers. Lattice defects can be created by irradiation with radioactive beams or by modifying the conditions of vapor deposition.

The negative-resistance semiconductor device prepared according to the invention can serve as a logic component or commutation component and is particularly useful in the field of computer circuits.

As can already be seen from what has been said hereinabove, it will be understood that the invention is not limited to the embodiments, or to the embodiments of its various parts, that have been more particularly envisaged. On the contrary, the invention includes all the variants.

FIG. 1



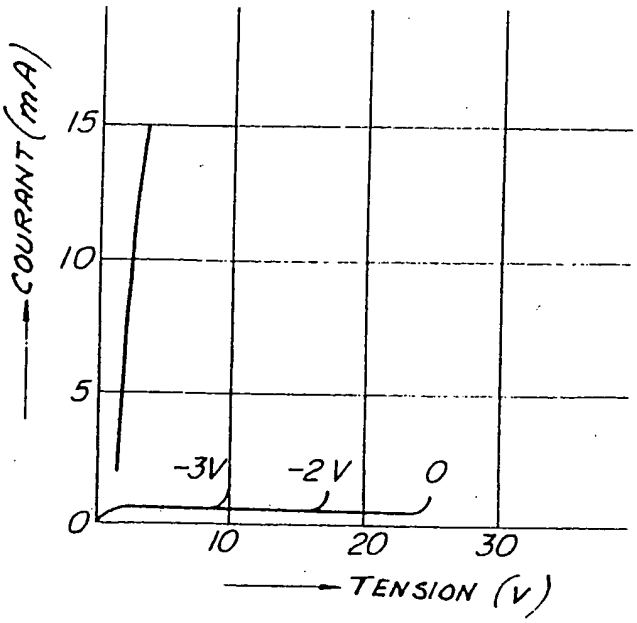


FIG. 2

FIG. 3